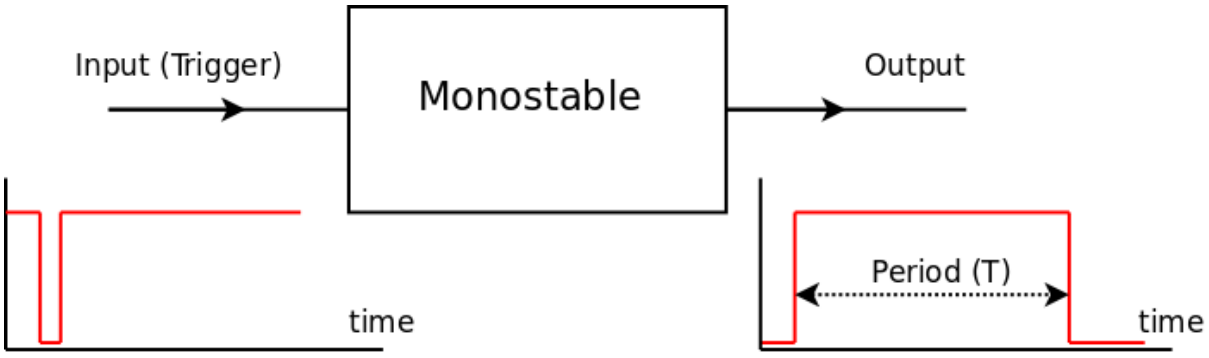
Monostable Circuits

Introduction

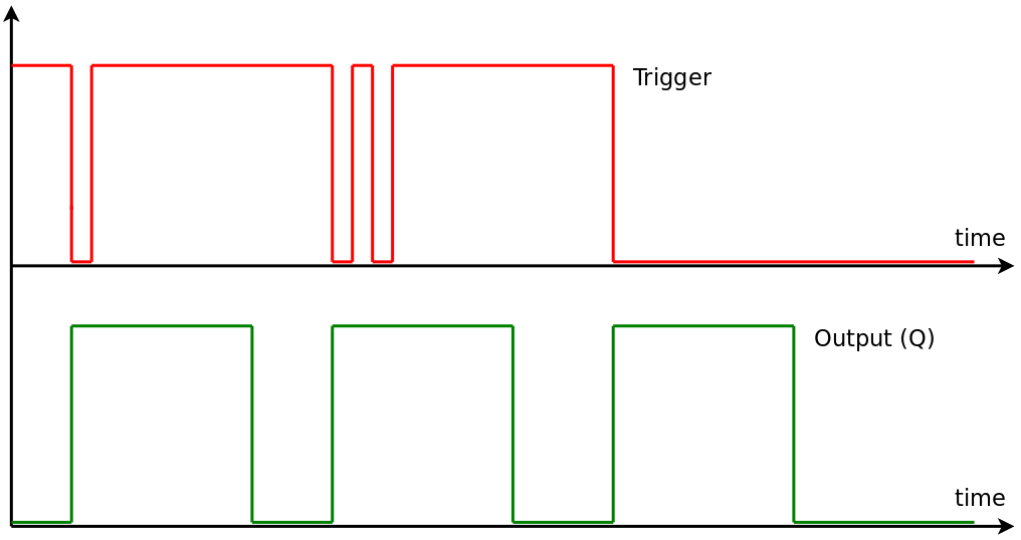
A monostable circuit is a digital circuit that is only stable in one state. This means that the output is usually LOW (logic 0) but it can be **triggered** and the output will go temporarily HIGH (logic 1) for some predetermined length of time. The HIGH state is not stable and eventually the output will go back to being LOW and will remain that way indefinitely unless forced to do otherwise. The length of time that the monostable stays in its unstable state is determined by external components such as capacitors and resistors. This time is called the Time Period (T).



The output is LOW until the monostable is triggered. At this point the output goes HIGH. The output stays HIGH for a set length of time (period = T) which is determined by the values of the resistor and capacitor that form part of the circuit.

The input is more unusual in that it is normally in a HIGH state and has to go LOW to trigger the monostable - this is called a falling edge.

Ideal Timing Diagram



The timing diagram shows the ideal behaviour of a monostable:

When the trigger goes LOW, the output immediately becomes HIGH. The monostable is triggered on the falling edge of the trigger input.

Even if there are multiple trigger falling edges, the output still only goes HIGH for the set time period from the first trigger's falling edge - the monostable is not 'restarted' by subsequent triggers.

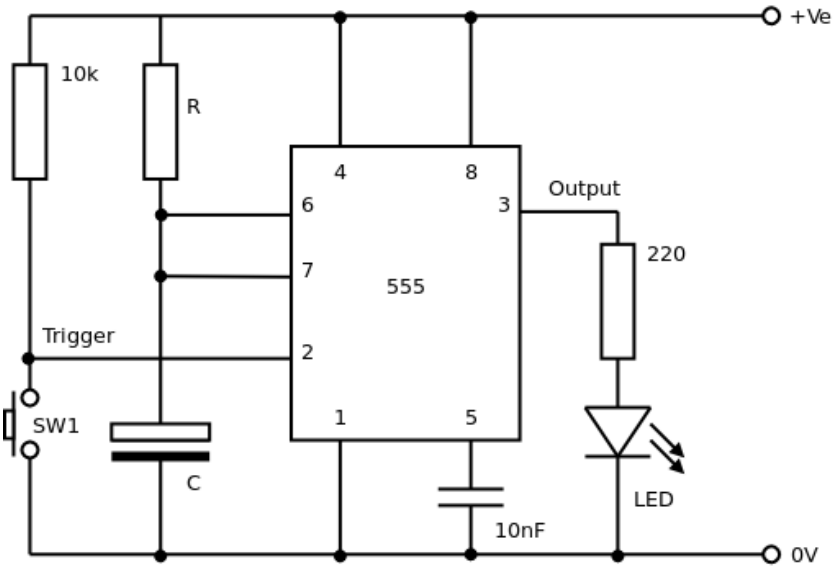
If the trigger stays low, the output still only stays HIGH for the set time period - holding the trigger LOW has no effect on the output.

Ideal Monostable

An ideal monostable should have the following properties:

- The time period starts as the trigger falls from HIGH to LOW
- The time period only depends on the values of the external components and is not affected by supply voltage
- Once the time period is started, further falling edges at the input should have no effect
- The time period should still be correct even if the input is held LOW for longer than the required time period
- The output should make a 'clean' single transition between logic states

The 555 based monostable



The 555 is an integrated circuit (IC) that can be used to make a convenient, if not necessarily very good, monostable.

The time period depends only on R and C such that:

$$T = 1.1 \times R \times C$$

In **normal operation** pin 4 is held HIGH. Pin 4 is the reset pin. When pin 4 is Logic 1 the 555 acts as a monostable. When pin 4 is Logic 0 the output remains LOW and the 555 does not act as a monostable

Pin 5 is connected through a 10 nF capacitor to 0 V.

Good points

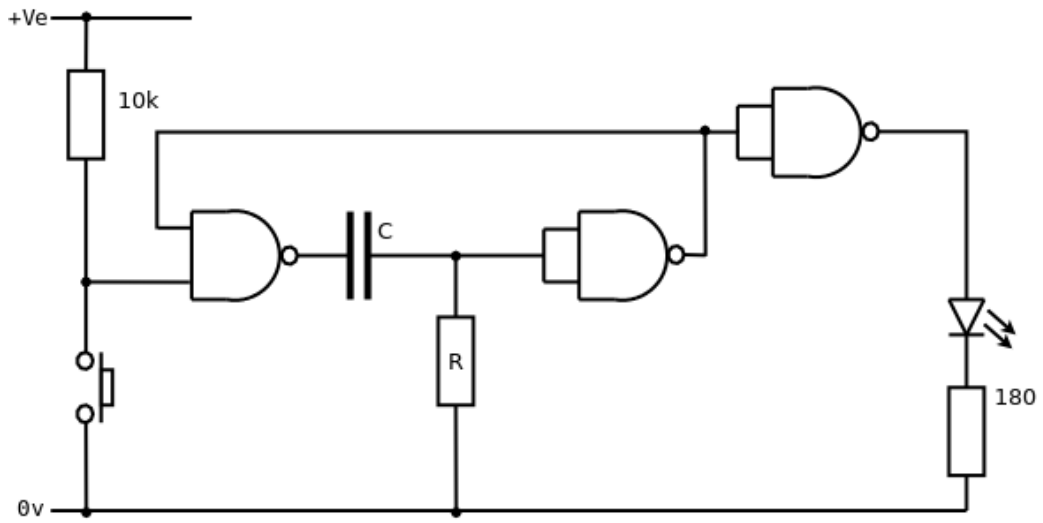
1. The 555 timer IC can be used to make a convenient monostable
2. The 555 IC can sink and source more current than the simple logic gates and therefore drive output transducers directly
3. The 555 IC, being an 8 Pin DIL package, is small and easier to construct than the NAND gate circuit

Bad points

1. The 555 monostable suffers from the fact that, if the trigger is held LOW for longer than the period of the monostable then the output stays HIGH and does not fall LOW as expected
2. The 555 IC can take a surge of current when the output changes. This can affect adjacent circuits. To overcome this a large value capacitor (47 µF) is used between pin 8 and pin 1 physically close to the IC itself (not shown)

The NAND gate monostable

The NAND gate monostable meets all of the criteria for a good monostable.



The output is represented by the LED which is usually OFF in the stable state.

The 10k resistor is a pull up resistor that keeps the input high unless the button is pressed.

Immediately the button is pressed, the capacitor which is uncharged in the stable state, begins to charge and hence the time period begins. The button has no further effect on the circuit until the output returns to its normal stable state.

The time period is determined by R and C and, for most logic gates, the time period is given by T = 0.7RC.

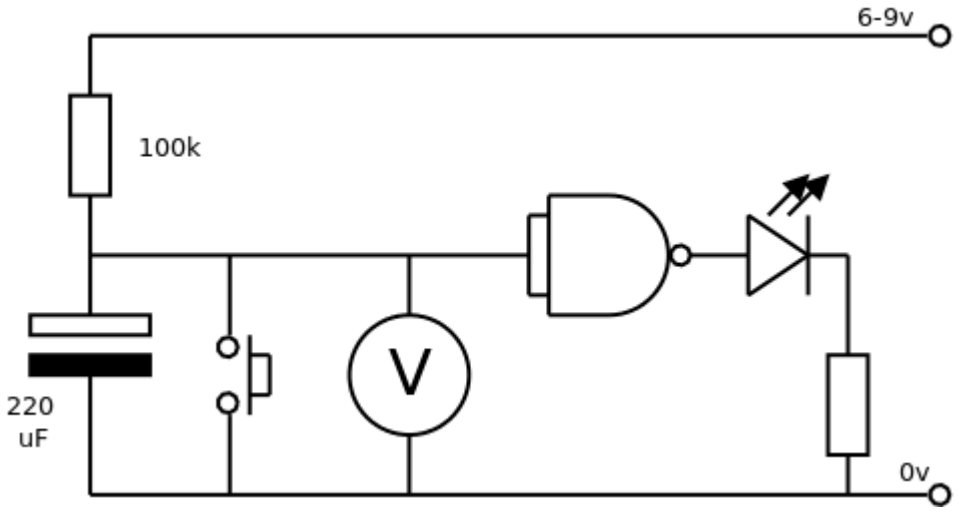
$$T = 0.7 \times R \times C$$

This is a very good monostable that behaves as it should but is harder to build and takes up more space on the circuit board.

Very Simple Monostable (do not use!)

The circuit shown is a very simple monostable, and not a very good one either!

It is useful to consider how it works as it helps to understand the more complex circuits



This is a poor circuit because:

- The capacitor discharging through the switch may cause damage.
- The time period starts when the button is released, not when it is pressed as required.
- The output can 'oscillate' as the voltage on the capacitor reaches the transition voltage of the gate
- The time period depends on what voltage the gate 'sees' the input as logic one or zero ... this depends on the type of gate used and so the time period depends on the type of gate used which it shouldn't.
- The time period can be 'restarted' by pressing the button before the output returns low ... this should not be possible.

Circuit Operation

It is important to remember that a capacitor, when it is charged, has a voltage across it and when it is not charged, it has no voltage across it. The capacitor charges through the resistor and so the rate at which it charges, and hence the time period, is determined by both the resistor and the capacitor values. Increasing either the resistor value or the capacitor value increases the time period.

In its stable state the capacitor is fully charged through the 100k resistor. The voltmeter reads full voltage (the supply voltage) which is logic 1.

Logic 1 at the input to the NAND gate, which is being used as a NOT gate, gives a logic zero on the output. This is the stable state.

When the button is pressed the capacitor is instantly discharged, the voltage at the input to the NAND gate falls to zero and hence the output rises to logic 1; this is the unstable state. The output stays at logic 1 as long as the button is pressed. Note: The discharge current through the button may be very high as you are effectively short circuiting the capacitor ... one reason why this is a poor circuit

When the button is released the capacitor will start to charge up slowly through the 100k resistor. The input to the NAND gate is still logic zero and so the output remains at logic 1.

After some time the capacitor will be charged enough so that the voltage across it now counts as logic 1 (as the capacitor charges, the voltage across it rises). Because the input is now logic 1 then the output falls to logic zero. As the capacitor charges up even more, the output stays at logic zero until the button is pressed again.

If we assume that the logic gate 'sees' a voltage of less than ½ the supply voltage as a logic zero, what will be the period of the monostable after the button is released? For a capacitor to reach half charge (and hence half supply voltage) it takes a time of 0.7RC. With the values shown this works out to be approx 15 seconds ... the actual time depends on at what point the gate 'switches' from logic 1 to logic 0.

$T = 0.7 \times R \times C = 0.7 \times 100 \times 10^{3} \times 220 \times 10^{-6} = 15.4$ seconds

Website

https://www.electronicsteaching.com/Electronics_Resources/DocumentIndex.html

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